

**FIG. 2**

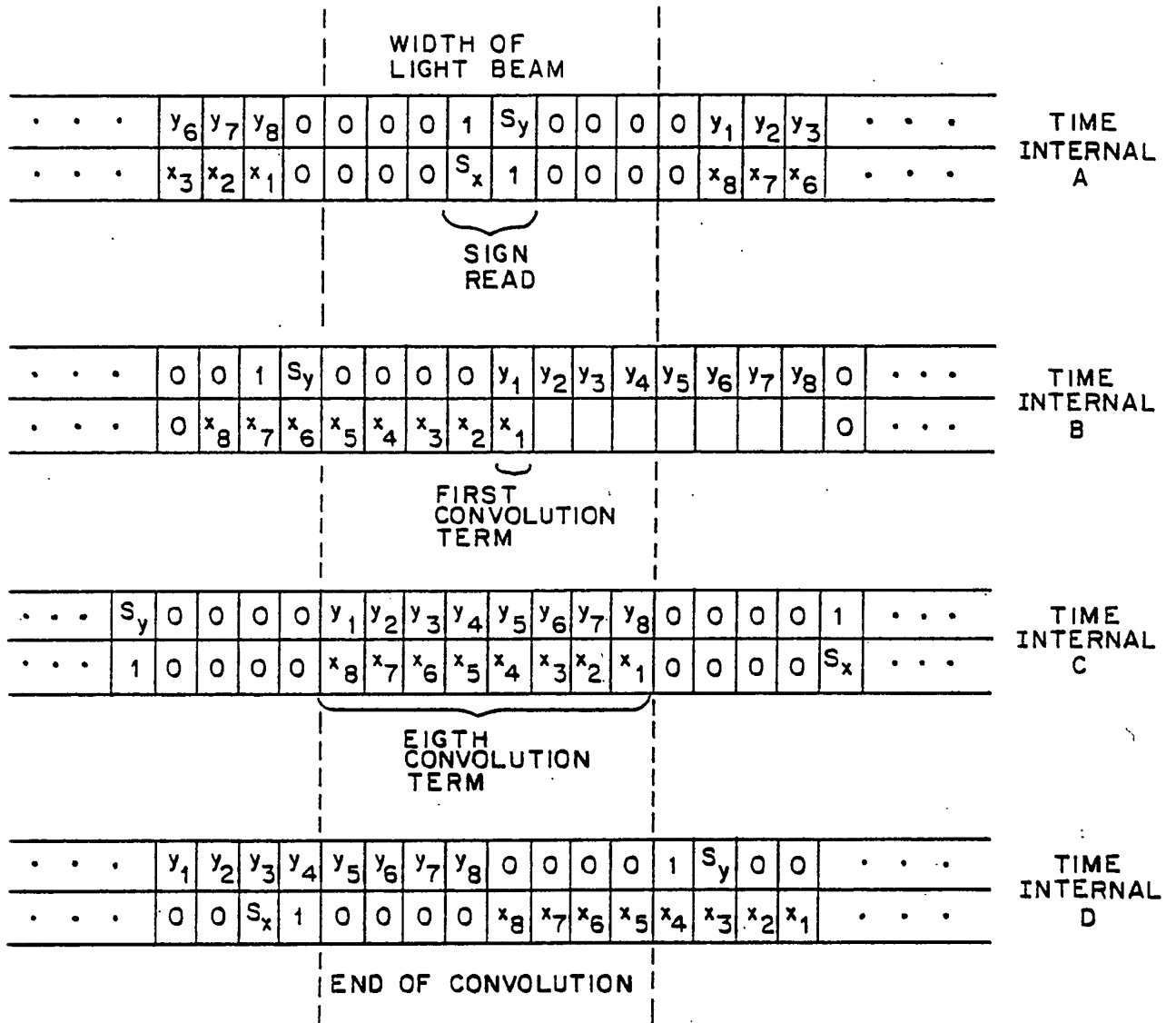


FIG. 3

$S_x$	$S_y$	$\Sigma$	CCD
0	0	0	+
0	1	1	-
1	0	1	-
1	1	2	+

FIG. 4A

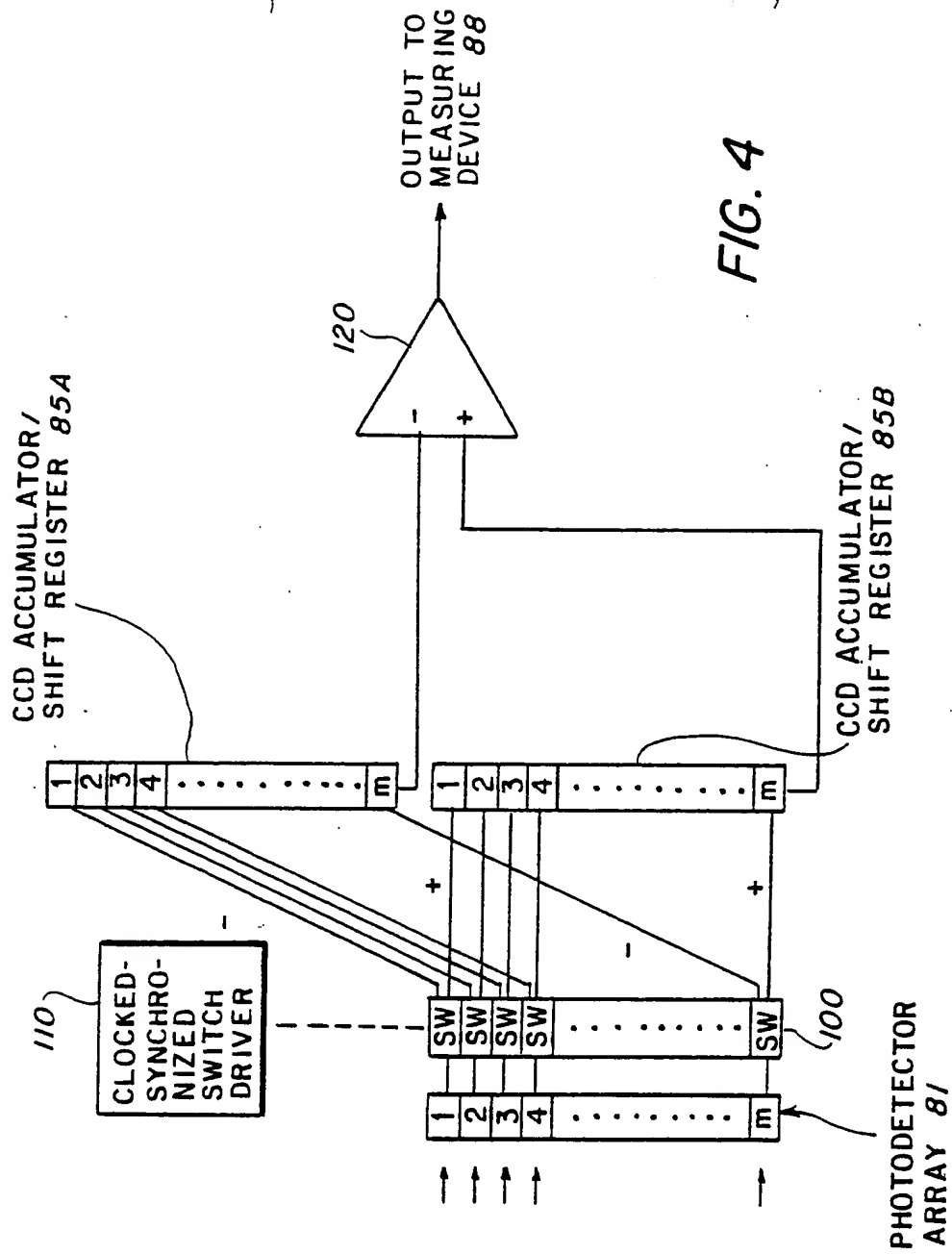


FIG. 4

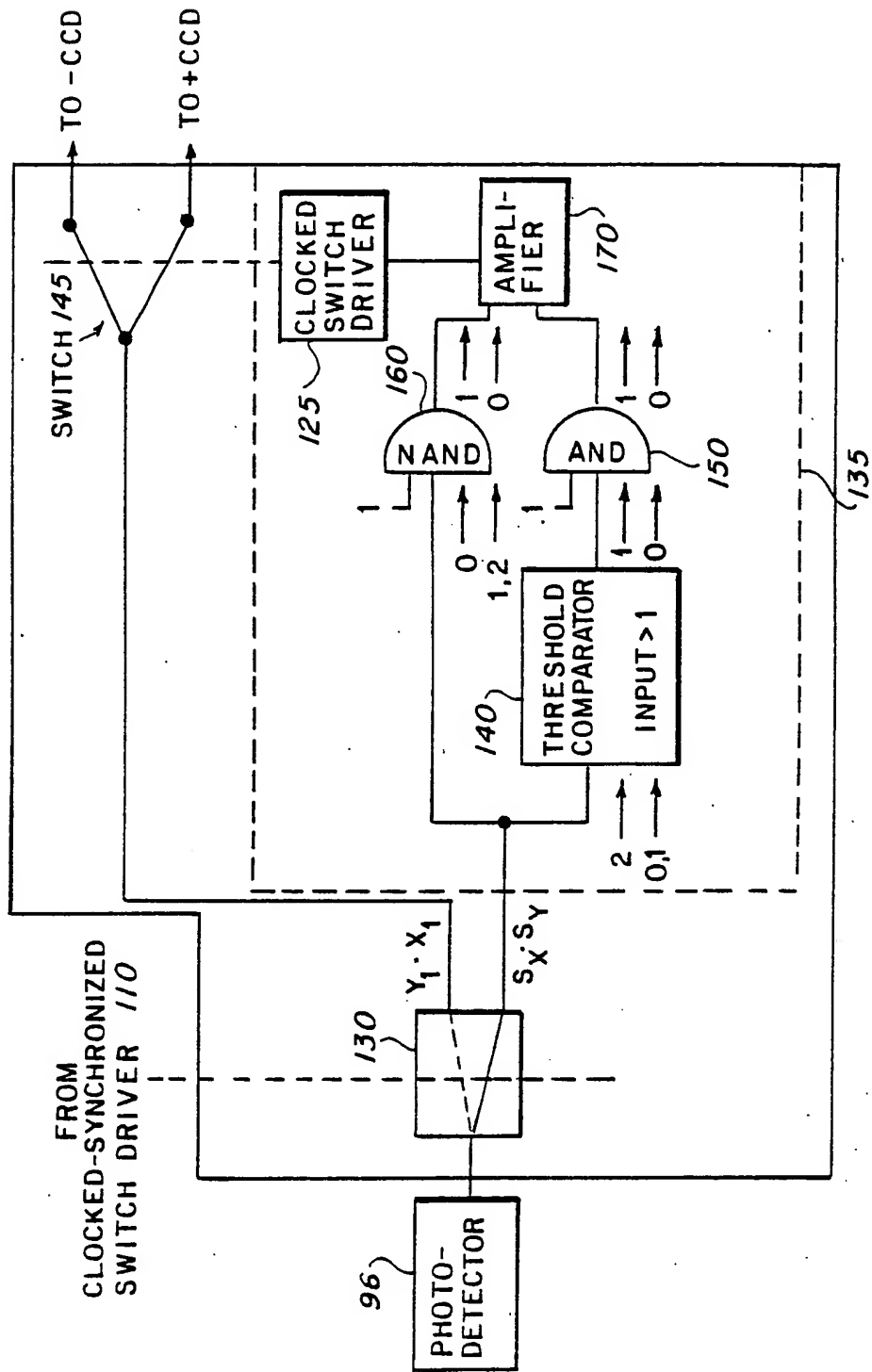
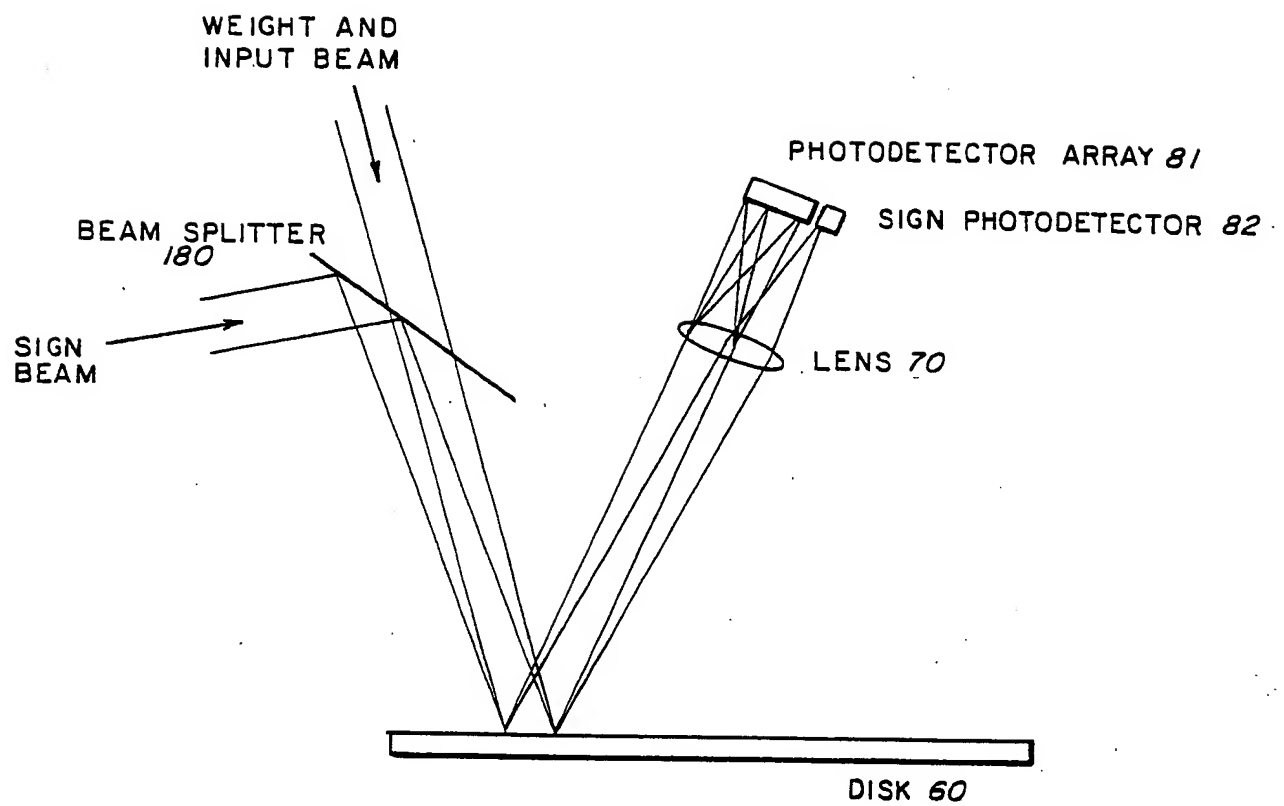


FIG. 5



**FIG. 6**



**FIG. 7**

# ANALOG AREA ENCODE INNER PRODUCT ARCHITECTURE

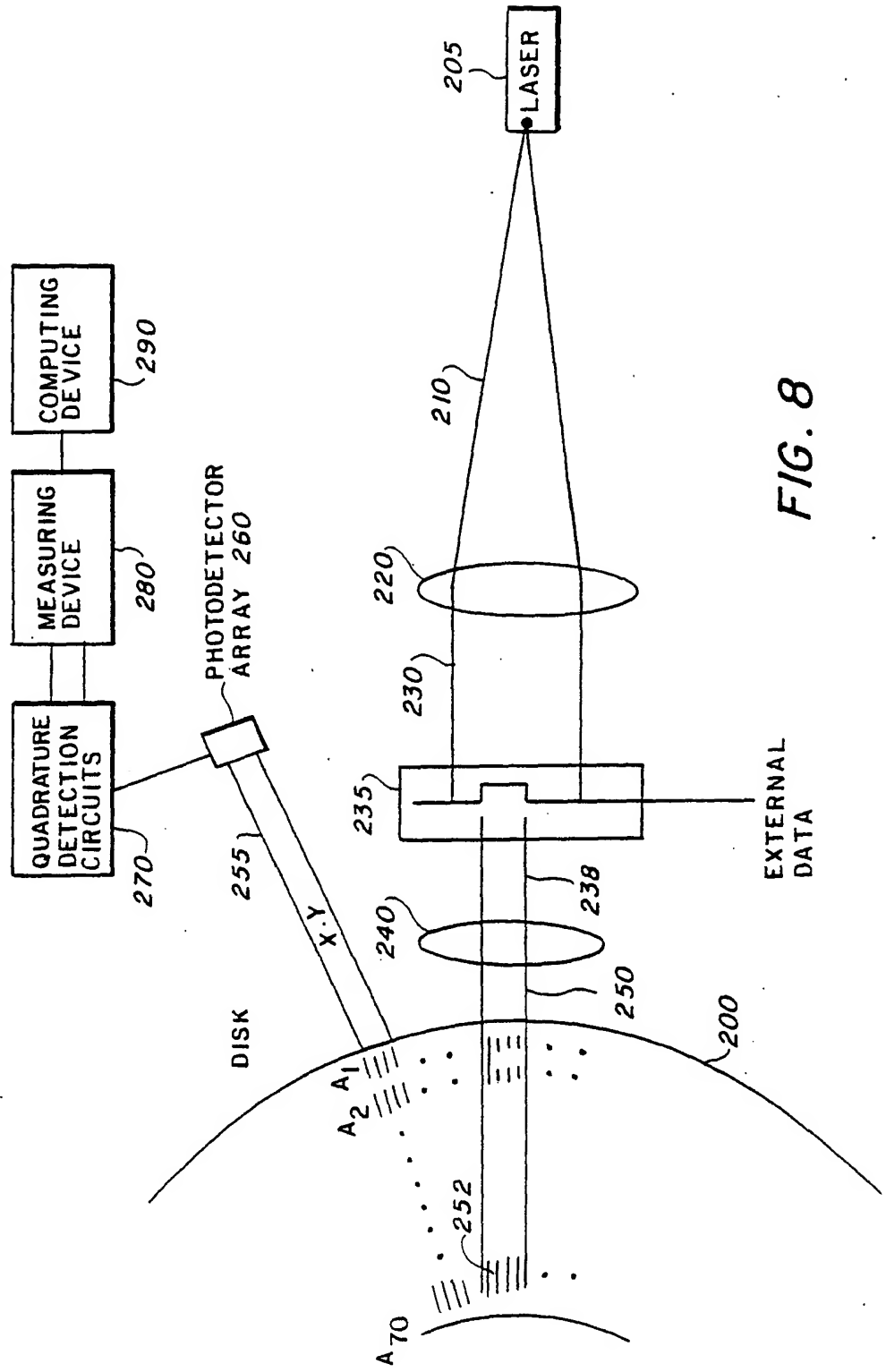


FIG. 8



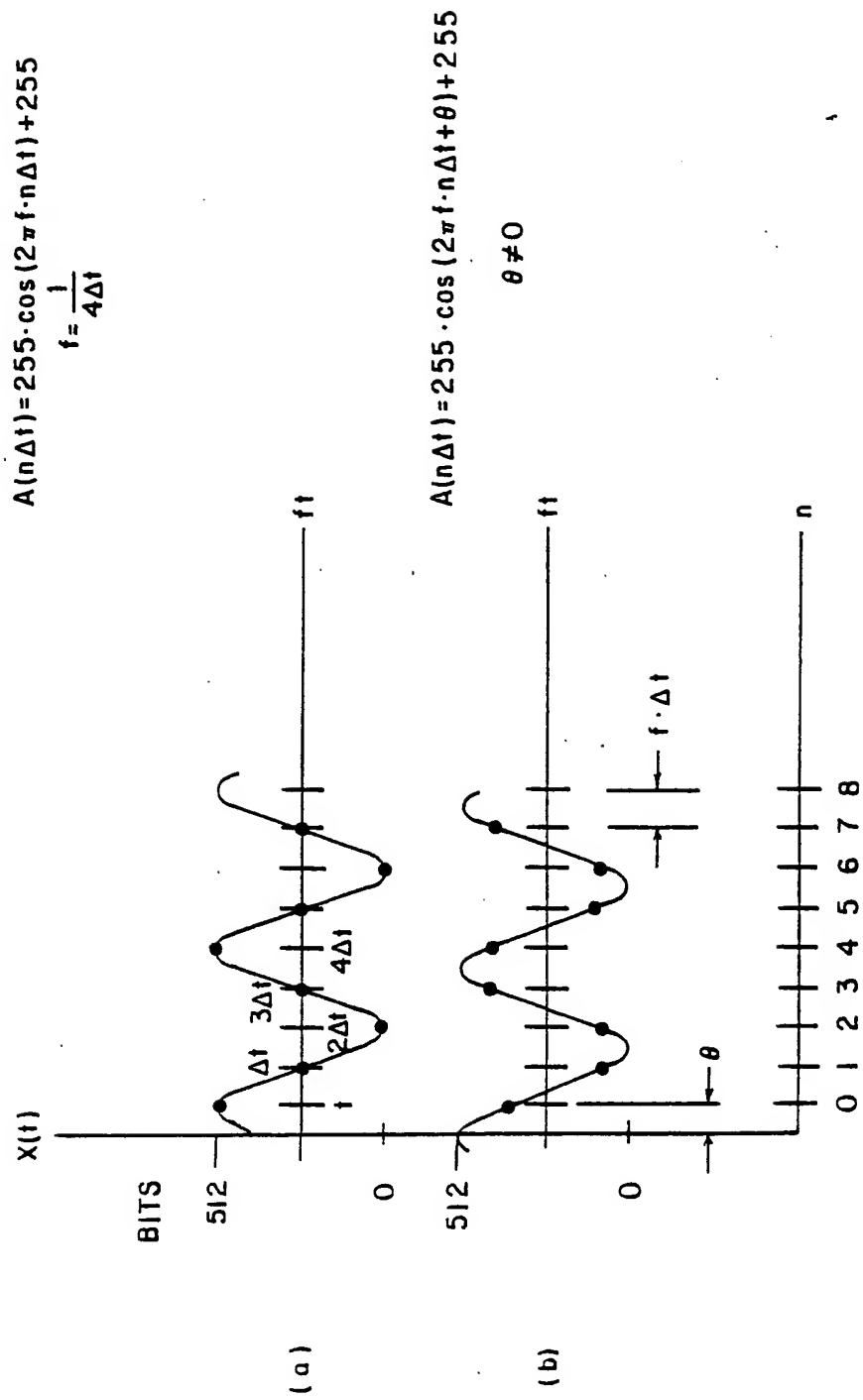
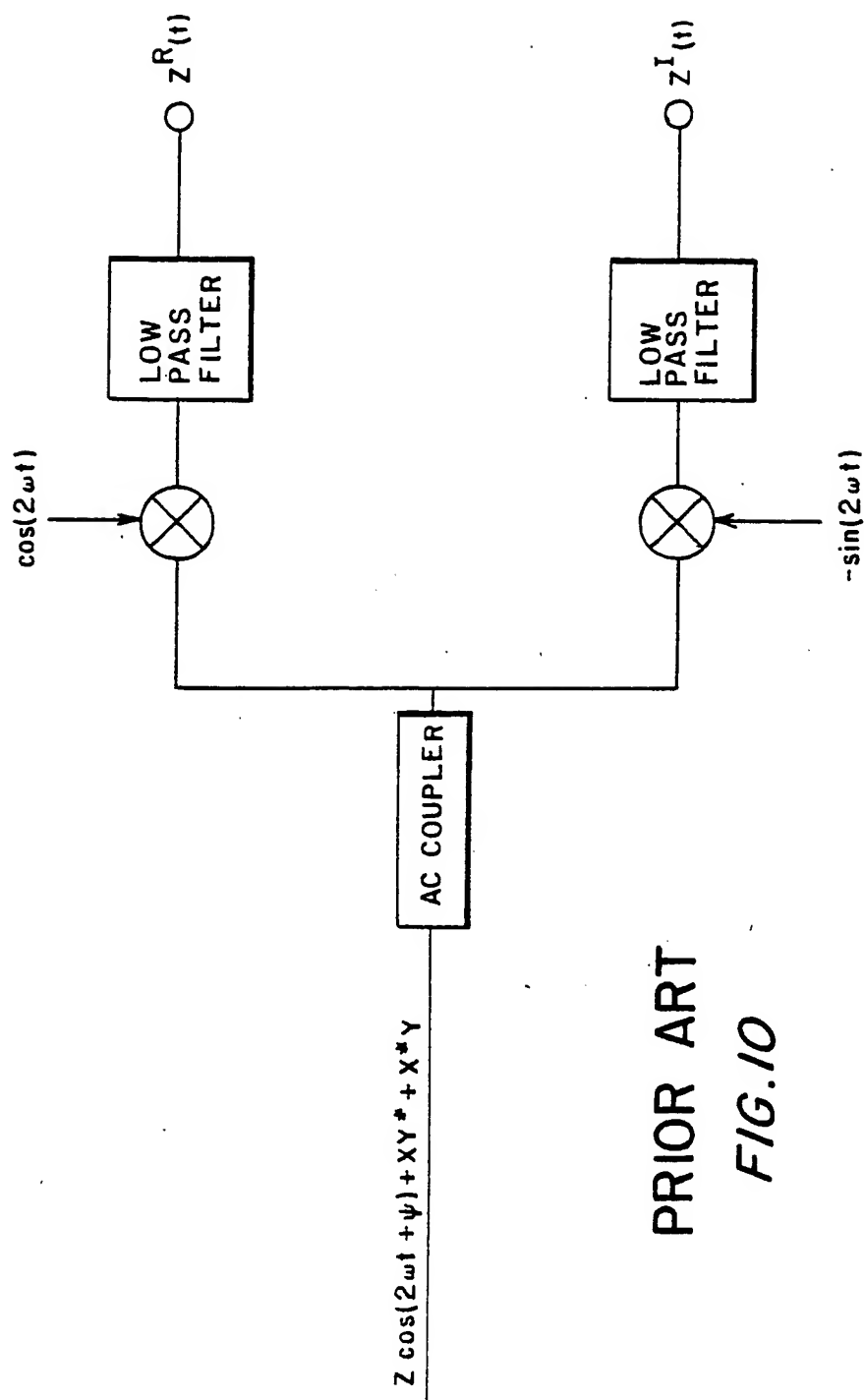


FIG. 9



PRIOR ART  
FIG.10